9/899957

L Number	Hits	Search Text	DB	Time stamp
1	67060	asymmetr$3	USPAT; US-PGPUB; JPO	2002/09/30 10:41
2	115566	implant$3	USPAT; US-PGPUB; JPO	2002/09/30 10:41
3	5275	(angle$1 or oblique$1 or degree$1) near10 implant$3	USPAT; US-PGPUB; JPO	2002/09/30 10:42
4	498648	gate$1	USPAT; US-PGPUB; JPO	2002/09/30 10:43
5	126148	source$1 same drain$1	USPAT; US-PGPUB; JPO	2002/09/30 10:43
6	19260	SOI or silicon adj2 insulat$3	USPAT; US-PGPUB; JPO	2002/09/30 10:43
7	171235	halo$1 or pocket$1	USPAT; US-PGPUB; JPO	2002/09/30 10:44
8	107356	gate$1 and (source$1 same drain$1)	USPAT; US-PGPUB; JPO	2002/09/30 10:44
9	1703	(gate$1 and (source$1 same drain$1)) and ((angle$1 or oblique$1 or degree$1) near10 implant$3)	USPAT; US-PGPUB; JPO	2002/09/30 10:45
10	67	((gate$1 and (source$1 same drain$1)) and ((angle$1 or oblique$1 or degree$1) near10 implant$3)) and (halo$1 or pocket$1) and (SOI or silicon adj2 insulat$3)	USPAT; US-PGPUB; JPO	2002/09/30 10:48
11	170	((gate$1 and (source$1 same drain$1)) and ((angle$1 or oblique$1 or degree$1) near10 implant$3)) and asymmetr$3	USPAT; US-PGPUB; JPO	2002/09/30 10:49
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	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	67060	asymmetr$3	USPAT; US-PGPUB; JPO	2002/09/30 10:41
2	BRS	L2	115566	implant$3	USPAT; US-PGPUB; JPO	2002/09/30 10:41
3	BRS	L3	5275	(angle$1 or oblique$1 or degree$1) near10 2	USPAT; US-PGPUB; JPO	2002/09/30 10:42
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7	BRS	L7	171235	halo$1 or pocket$1	USPAT; US-PGPUB; JPO	2002/09/30 10:44
8	BRS	L8	107356	4 and 5	USPAT; US-PGPUB; JPO	2002/09/30 10:44
9	BRS	L9	1703	8 and 3	USPAT; US-PGPUB; JPO	2002/09/30 10:45
10	BRS	L10	67	9 and 7 and 6	USPAT; US-PGPUB; JPO	2002/09/30 10:48
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12	BRS	L12	14	11 and 7 and 6	USPAT; US-PGPUB; JPO	2002/09/30 10:55
13	BRS	L14	1912	1 and 8	USPAT; US-PGPUB; JPO	2002/09/30 10:56
14	BRS	L15	230	6 and 14	USPAT; US-PGPUB; JPO	2002/09/30 10:56
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16	BRS	L19	6530	(dummy or sacrificial or mandrel$1) same 4	USPAT; US-PGPUB; JPO	2002/09/30 11:10
17	BRS	L20	210	19 and 3	USPAT; US-PGPUB; JPO	2002/09/30 11:10
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19	BRS	L22	49	21 not 16	USPAT; US-PGPUB; JPO	2002/09/30 11:14
20	BRS	L23	159	20 not 21	USPAT; US-PGPUB; JPO	2002/09/30 11:45
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23	BRS	L42	301	3 and 1	USPAT; US-PGPUB; JPO	2002/09/30 11:46

Article 1 of 10

TITLE Sacrificial Silicon Sidewall for **Damascene Gate** Formation. November 2000.

SECURITY IBM CONFIDENTIAL

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LOCATION East Fishkill

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AUTHOR Burns, S. M. Hanafi, H. I.

REPORT Docket- FIS919990161

ABSTRACT 15p. A method of fabricating MOSFET devices in which the gate polysilicon is not consumed during damascene etch back, comprising (a) forming a gate stack on a surface of a silicon-containing substrate, said gate stack having at least a pad oxide layer formed on said surface of said silicon-containing substrate and a nitride layer formed on said pad oxide layer; (b) forming a trough in said gate stack stopping on said pad oxide layer exposing a portion of said pad oxide layer, said trough having vertical sidewalls; (c) forming a conformal silicon layer on said gate stack and in said trough, including said vertical sidewalls and said exposed pad oxide layer; (d) removing the conformal silicon layer from said gate stack and said exposed pad oxide layer whereby silicon remains on the vertical sidewalls of said trough; (e) removing the exposed pad oxide from said trough exposing a portion of the silicon-containing substrate; (f) oxidizing the silicon on said vertical sidewalls of the trough and in said exposed silicon-containing substrate forming oxide layers in said vertical sidewalls and on said exposed silicon-containing substrate; (g) forming doped polysilicon in said trough; (h) performing a second oxidation step in which an oxide layer is formed on a top surface of said doped polysilicon; (i) removing the remaining nitride layer of the gate stack forming a gate region which is protected on all sides by oxides; and (j) forming source and drain regions in said silicon-containing substrate.

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Article 1 of 2

TITLE	A study of 100 nm channel length **asymmetric** channel MOSFET by using charge pumping
DOCNO	INS 994701324
AUTHOR	Mahapatra, S. Ramgopal Rao, V. Parikh, C.D. **Vasi**, J. Cheng, B. Woo, J.C.S.
CORPAUTH	Dept. of Electr. Eng., Indian Inst. of Technol., Bombay, Indi:
PUBLISHR	Elsevier
CODEN	MIENEF
ISSN	0167-9317
ORDER	Microelectron. Eng. (Netherlands) Vol.48, No.1-4 Sept. 1999 P193-6
CONFRNCE	11th Biennial Conference on Insulating Films on Semiconductors Koster Banz, Germany 16-19 June 1999
ABSTRACT	Lateral **Asymmetric** Channel (LAC) MOSFETs with channel lengths down to 0.1 mu m have been fabricated and characterized for their electrical performance. Using charge pumping, we show, for the first time, channel V/sub T/ profiles obtained experimentally, demonstrating realization of **asymmetric** channel MOSFETs down to 0.1 mu m channel lengths. Our detailed experimental characterizations show improved performance for LAC MOSFETs over conventional MOSFETs, in addition to excellent hot carrier reliability. Based on 2-D device simulation results, we attribute the improved hot carrier reliability in LAC MOSFETs to the reduced peak lateral electric field in the channel.
CLASCODE	B2560R
SUBJHEAD	hot carriers MOSFET semiconductor device reliability
ABSTNUM	B2000-01-2560R 031
RECTYPE	06
TRMTCODE	X

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Article 3 of 3

TITLE	The graded channel SOI MOSFET to alleviate the parasitic bipolar effects and improve the output characteristics
DOCNO	INS 003206419
AUTHOR	**Pavanello,** M.A. Martino, J.A. Dessard, V. Flandre, D.
CORPAUTH	Lab. de Sistemas Integravels, Sao Paulo Univ., Brazil
PUBLISHR	Electrochem. Soc
PUBADDR	Pennington, NJ, USA
ORDER	Proceedings of the Ninth International Symposium on Silicon on Insulator Technology and Devices. (Electrochemical Society Proceedings Vol.99-3) 1999 P293-8
CONFRNCE	Proceedings of Silicon on Insulator Technology and Devices Seattle, WA, USA 2-7 May 1999
ISBN	1 56677 225 7
ABSTRACT	A new SOI MOSFET structure based on an **asymmetric** doping profile in the body is proposed for the first time with the goal of alleviating the inherent parasitic bipolar effect in fully depleted SOI MOSFETs and improving the output conductance.
CLASCODE	B2560R B2530F B2550B B2560B
SUBJHEAD	doping profiles electric admittance MOSFET semiconductor device measurement semiconductor device models silicon on insulator
ABSTNUM	B2000-09-2560R 123
RECTYPE	06
TRMTCODE	P T X

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Article 1 of 3

TITLE	Graded channel fully depleted silicon on insulator nMOSFET for reducing the parasitic bipolar effects
DOCNO	INS 002104968
AUTHOR	**Pavanello,** M.A. Martino, J.A. Flandre, D.
CORPAUTH	Lab. de Sistemas Integraveis, Escola Politecnica da Univ. de Sao Paulo, Brazil
PUBLISHR	Elsevier
CODEN	SSELA5
ISSN	0038-1101
ORDER	Solid State Electron. (UK) Vol.44, No.6 June 2000 P917-22
ABSTRACT	An extended study of the occurrence of inherent parasitic bipolar effects in conventional and graded channel fully depleted silicon on insulator nMOSFETs is carried out. The graded channel device is a new **asymmetric** channel MOSFET, fabricated through a simple process variation. Measurements and two dimensional simulations are used to demonstrate that the graded channel device efficiently alleviates the parasitic BJT action, improving the breakdown voltage, by the reduction of impact ionization in the high electric field region. Based on process/device simulation and modeling, the multiplication factor and parasitic bipolar gain, which are the responsible parameters for the parasitic BJT action, are investigated separately providing a physical explanation. The abnormal subthreshold slope and hysteresis phenomenon are also studied and compared.
CLASCODE	B2560R B2560B B2550X
SUBJHEAD	elemental semiconductors impact ionisation MOSFET semiconductor device breakdown semiconductor device measurement semiconductor device models semiconductor process modelling silicon silicon on insulator
ABSTNUM	B2000-07-2560R 019
RECTYPE	02
TRMTCODE	P T X

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Article 5 of 10

TITLE	Plasma damage free gate process using chemical mechanical polishing for 0.1 mu m MOSFETs
DOCNO	INS 992601541
AUTHOR	Saito, T. Yagishita, A. Inumiya, S. Nakajima, K. Akasaka, Y. Ozawa, Y. Yano, H. Hieda, K. Suguro, K. Arikado, T. Okumura, K.
CORPAUTH	Microelectron. Eng. Lab., Toshiba Corp., Yokohama, Japan
PUBLISHR	Publication Office, Japanese Journal Appl. Phys
CODEN	JAPNDE
ISSN	0021-4922
ORDER	Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) Vol.38, No.4B April 1999 P2227-31
CONFRNCE	Proceedings of the 1998 International Conference on Solid State Devices and Materials (SSDM'98) Hiroshima, Japan 7-10 Sept. 1998
ABSTRACT	We propose a new transistor process called the **Damascene gate** process, where in a gate electrode is patterned by chemical mechanical polishing (CMP). In this process, source/drain implants are carried out by using a dummy gate pattern as a mask and activation annealing is completed before the actual gate oxide formation. After removal of the dummy gate, fresh oxide and gate electrode films are formed in grooves and the gate electrode film is patterned by CMP. As a result. The gate electrode surface is completely planarized and the sheet resistivity of the gate electrode is very uniform in a line width range from 0.2 mu m to 5 mu m. Metal oxide semiconductor field effect transistors (MOSFETs) formed by the **Damascene gate** process were found to show higher electron mobility, smaller threshold voltage deviation and lower subthreshold swing due to lower surface state density as compared with conventional transistors. Therefore, the **Damascene gate** process is promising for the fabrication of sub quarter micron MOSFETs.
CLASCODE	B2560R B2550E
SUBJHEAD	chemical mechanical polishing MOSFET
ABSTNUM	B1999-08-2560R 027
RECTYPE	06
TRMTCODE	P X

DAMASCENE-GATE THIN FILM TRANSISTORS WITH ULTRA-THIN GATE DIELECTRICS

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The push towards larger and higher resolution flat panel displays requires an improvement in current thin-film transistor (TFT) performance. Devices should have lower threshold voltages, sub-threshold slopes and, in particular, lower gate line resistances if large, high-resolution, video-quality displays are to be realized. This can be achieved by using thicker gate lines and thinner gate dielectrics. However, since amorphous silicon TFTs currently being used in active-matrix liquid crystal displays are bottom-gate structures, there is the problem of step coverage. Specifically, a thick gate dielectric is required to adequately cover the gate metal in order to prevent leakage current between the gate and the source/drain.

The approach presented in this paper is to embed the gate metal into a trench made into a silicon nitride passivating layer above the substrate so that the top of the gate metal is level with the surface of the passivating layer. This damascene-gate structure has several advantages: (1) reduces gate line resistance by allowing for thick gate lines, (2) allows the use of low-resistivity metals such as copper which would be encapsulated by the silicon nitride sidewalls and a metal cap-layer, and (3) permits the use of thin gate dielectrics (< 200 nm).

Damascene-gate TFTs (dTFTs) were fabricated on Corning 7059 glass substrates coated with a 500 nm SiN passivation layer. Trenches from 150 nm to as deep as 300 nm were etched into this passivation layer using RIE, patterned using a photoresist etch mask. The photoresist etch mask remains, and gate metal was then e-beam evaporated to a thickness equal to the depth of the trench. Gate metal not in the trench is then lifted-off. There is no chemical-mechanical polishing (CMP) step. Dektak profilometry shown in Fig. 1 reveals that the surface topology is quite smooth with mismatch between the top of the gate and the top of the surrounding passivation layer typically around 10 nm.

SiN gate insulators of thicknesses 280 nm, 180 nm, 140 nm, 90 nm and 50 nm were deposited on top of these damascene gates. The active and doped layers are intrinsic and n^+ amorphous silicon of thicknesses 160 nm and 50 nm, respectively. The source/drain metal is 100 nm of e-beam evaporated Cr. All films were grown using a multi-chamber RF-PECVD system.

To examine whether the encapsulation ability of these damascene-gate structures can be used in conjunction with copper gate lines, two gate metal configurations were used for the 140 nm thick gate dielectric devices: Cr only, and Cu with a 30 nm Cr cap-layer. Use of Cu gate lines would dramatically reduce gate line resistance in active-matrix displays, since the resistivity of Cu is 20 times smaller than Cr and 14 times smaller than Mo-Ta. Fig. 2 shows that dTFTs with Cr-capped Cu gates can be fabricated with device performances comparable to those made with all-Cr gates.

As the data in Figs. 3 and 4 illustrate, both the threshold voltage and the sub-threshold slope decrease with a decrease in gate dielectric thickness as expected. In addition, the data also indicate that this is achieved without sacrificing mobility or breakdown field strength. The damascene gate structure makes such improvements in device performance possible by its use of an embedded gate and thin gate dielectric.

The authors would like to acknowledge DARPA and PPL for their support of this research.

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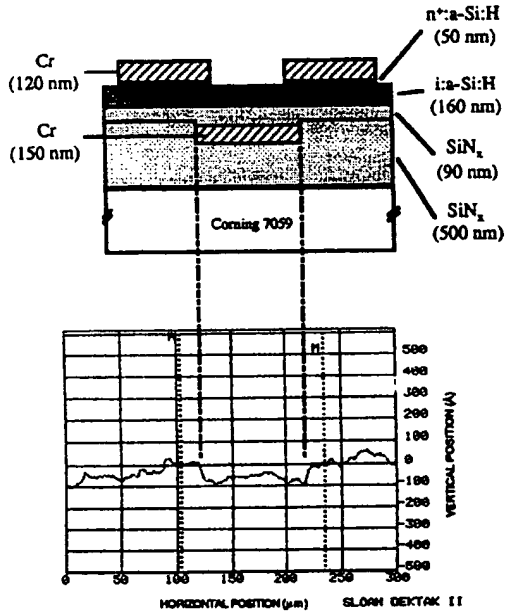

Fig. 1. Cross-sectional schematic of a dTFT and a Dektak profilometer measurement over the gate region prior to gate dielectric deposition.

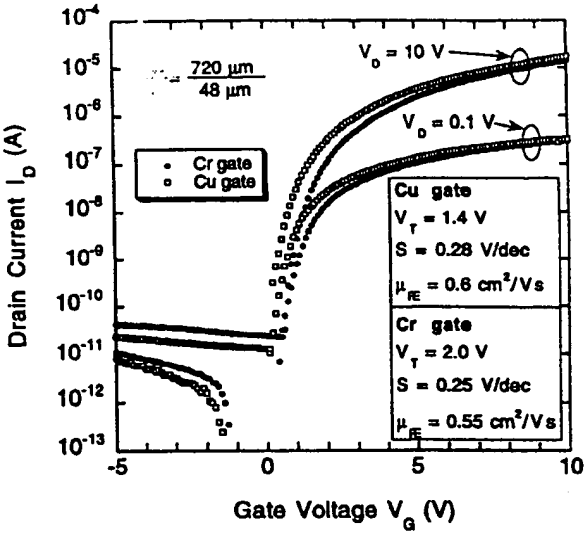

Fig. 2. Transfer characteristics for dTFTs with 140 nm thick gate dielectrics, comparing two kinds of gate metal: (●) 150 nm thick Cr gate and (□) 130 nm Cu gate capped with 30 nm of Cr.

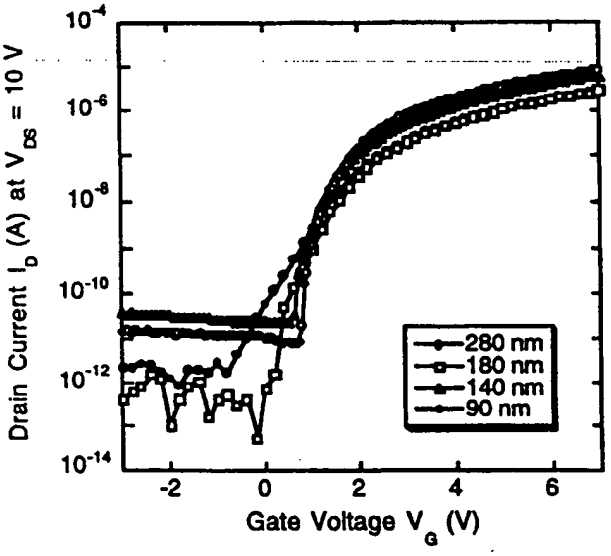

Fig. 3. Transfer characteristics for dTFTs of various gate dielectric thicknesses.

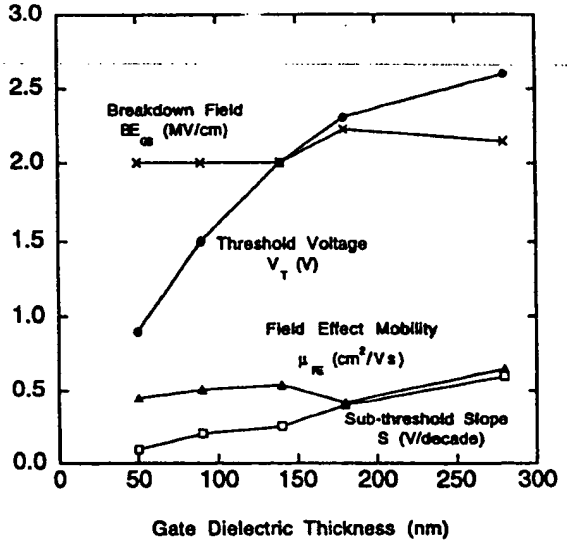

Fig. 4. Performance metrics for dTFTs as a function of gate dielectric thickness.

as the difference between extracted and imposed values (in absolute value) normalized to the imposed value. As can be seen, τ_g and s_0 errors vary with L_g in opposite ways. s_0 data confirm the analysis of Vanstraelen *et al.* [1], in that accurate s_0 extraction requires L_g not to be too long. Increasing L_g has, instead, a beneficial effect on τ_g accuracy, as both effects (1) and (2) described above are confined to regions which becomes less and less important with respect to the increasing gate depletion volume. As a result, τ_g and s_0 can be evaluated from the same structure with acceptable accuracy only in correspondence of a trade-off value of L_g.

Another aspect to point out is that both s_0 and τ_g errors are influenced by the τ_g value, as clearly shown by Fig. 4. A lower τ_g, means indeed higher lateral current flow when the gate is operated in depletion, determining, for a given gate length, a greater quasi-Fermi potential change under the gate. This results in lower s_0 accuracy. As far as τ_g accuracy is concerned, a lower τ_g value leads to a higher bulk generation current beneath the gate, thus making the relative importance of effects (1) and (2) lesser. This, in turn, allows for a better τ_g accuracy. As a result, the trade-off value of L_g depends on τ_g, as clearly evident from Fig. 4. This is also true with respect to s_0, which, as shown in Fig. 3, impacts τ_g extraction accuracy, and to other technological parameters such as N_B and N_{ox}, whose effect is not shown here.

IV. Conclusions

The intrinsic limits to the accuracy with which bulk generation lifetime and surface generation velocity can be measured in high-resistivity silicon using a gated diode have been investigated. Practical consequence of what evidenced is that the gated diode layout, and specifically the gate length, needs to be carefully tailored to extract, with acceptable accuracy, both τ_g and s_0 from the same device. Alternatively, two different test structures, one having a "short" L_g, the other with a "long" L_g, need to be used to separately evaluate s_0 and τ_g. The latter approach appears to be preferable in all cases where the values of the different technological parameters affecting extraction precision are not known with sufficient accuracy at the layout-design stage, or such parameters are expected to vary significantly during the device lifetime, as, for instance, when the gated diode is used to monitor changes in τ_g and/or s_0 induced by electrical stress or radiation.

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An 0.1-μm Asymmetric Halo by Large-Angle-Tilt Implant (AHLATI) MOSFET for High Performance and Reliability

Hyungsoon Shin and Seungjun Lee

***Abstract*—A new 0.1-μm MOSFET structure called asymmetric halo by large-angle-tilt implant (AHLATI) is proposed for substantial reduction of short-channel and hot-carrier effects while enhancing the current driving capability. This structure differs from the conventional devices in that it has an asymmetric channel profile with a localized pileup region next to the source junction.**

***Index Terms*—Hot carriers, integrated circuit doping, MOSFET's.**

I. Introduction

There have been intensive studies into 0.1-μm MOSFET devices [1]–[3]. One of the key challenges in scaling the MOSFET into a 0.1-μm regime is maintaining good short-channel behavior without speed penalty. Recently, it was reported that the V_{th} roll-off effect and subthreshold leakage current can be reduced by locally raising the channel doping next to the source/drain (S/D) junctions [4], [5]. Another important physical phenomenon which should be considered in order to improve the performance of 0.1-μm MOSFET's is the velocity overshoot effect. In order to take full advantage of the drain current enhancement due to velocity overshoot, the importance of the spatial gradient of the electric field at the source end of the channel was suggested by using hydrodynamic (HD) and Monte Carlo simulators [6], [7].

The purpose of this letter is to describe a new structural concept for 0.1-μm MOSFET's which substantially reduces short-channel effect and enhances the device performance while retaining manufacturability. This new structure (AHLATI) differs markedly from the conventional type of MOSFET structure in that the channel profile is laterally nonuniform with a localized pileup region next to the source junction, as shown in Fig. 1. The conventional and AHLATI structures have a gate oxide thickness of 4 nm and punchthrough-stop implant of 40 keV boron with a dose of 4×10^{12} cm^{-2}. The processing sequence of AHLATI is the same as that of the conventional device except for the V_{th} adjustment implant. The conventional device has a uniform channel profile in the lateral direction and the 90-keV BF_2 ions at a dose of 8×10^{12} cm^{-2} were implanted to adjust the V_{th} before gate electrode formation. In comparison, the asymmetric channel profile for AHLATI was formed by the V_{th} adjustment implant with appropriate orientation after gate electrode formation. For such a channel profile shown in Fig. 1, the 60-keV BF_2 ions at a dose of 1×10^{13} cm^{-2} were implanted with a

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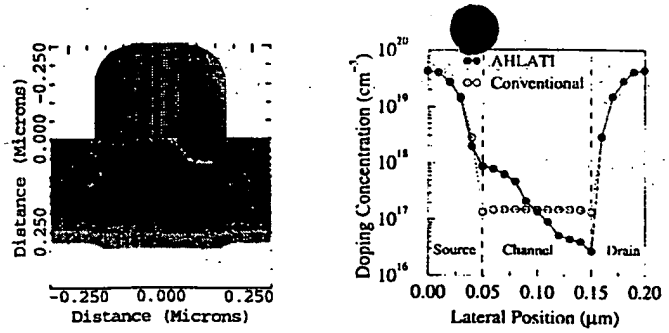

Fig. 1. (a) AHLATI (asymmetric halo by large-angle-tilt implant) structure and (b) lateral impurity profiles along the Si/SiO_2 interface for AHLATI and conventional NMOSFET's with $L_{eff} = 0.1$ μm.

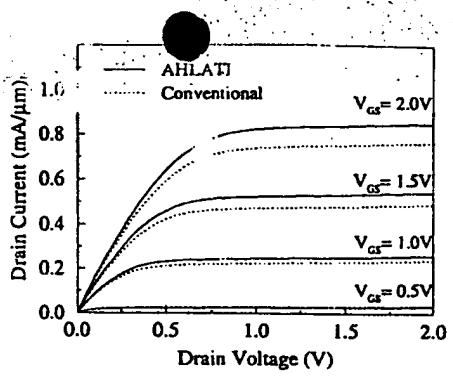

Fig. 3. I_D–V_D characteristics of AHLATI and conventional NMOSFET's with $L_{eff} = 0.1$ μm.

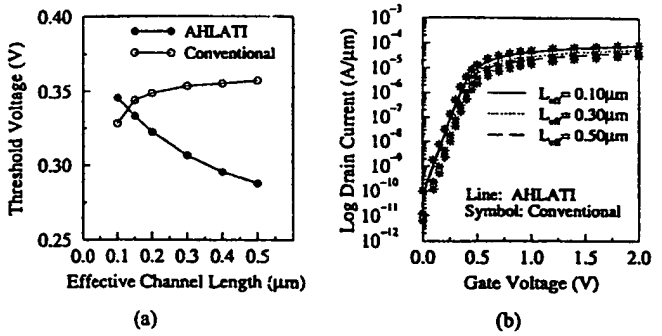

Fig. 2. (a) Threshold voltages and (b) subthreshold characteristics as a function of effective channel length for AHLATI and conventional NMOSFET's. The threshold voltage is defined as the gate voltage for the drain current of $W_{eff}/L_{eff} \cdot 10^{-7}$ A ($V_{DS} = 0.05$ V).

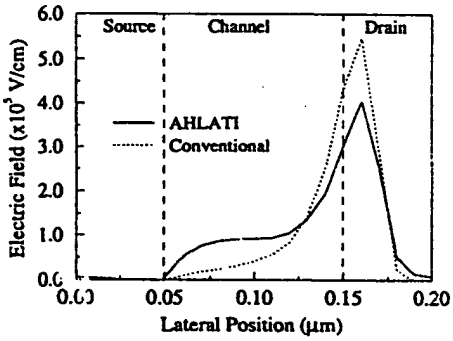

Fig. 4. Simulated electric fields along the channel for AHLATI and conventional NMOSFET's with $L_{eff} = 0.1$ μm ($V_{DS} = V_{GS} = 2.0$ V).

tilt-angle of 60°. After gate electrode formation, 40-keV As ions at a dose of 2×10^{14} cm^{-2} were implanted to form the shallow S/D extensions. After 1000 Å sidewall formation, the deep S/D junctions are formed with an As dose of 5×10^{15} cm^{-2} at 40 keV, followed by rapid thermal annealing at 1050 °C for 10 s.

To optimize the energy, dose, and tilt-angle of the V_{th} adjustment implantation for the AHLATI structure, extensive process and device simulations have been performed using the well-known TSUPREM4 [8] and MEDICI [9] simulators. The implantation condition was determined to locate the peak of the localized pileup region just next to the source junction at the Si/SiO_2 interface, which is required to produce the channel length independent subthreshold characteristics and maximize the drain current enhancement due to velocity overshoot [5], [7]. This implant condition is different from the published structures [10], [11] with pocket implant, where the conditions of pocket implant were determined to locate the peak concentration near to the S/D junction depth for the reduction of bulk-punchthrough effect. Fig. 2 shows V_{th} and subthreshold characteristics as a function of effective channel length (L_{eff}) for both AHLATI and conventional devices. AHLATI shows improved short-channel effect (reverse short-channel effect and channel length independent subthreshold characteristics), because the high boron concentration at the source side limits the subthreshold current of MOSFET.

The I–V characteristics for AHLATI and conventional devices with L_{eff} of 0.1 μm are compared in Fig. 3. Even if V_{th} of AHLATI is larger than that of the conventional device (Fig. 2), AHLATI shows larger drain current than that of the conventional device (Fig. 3). In addition, it was found that I_{off} of AHLATI is smaller than that of the conventional device. To find out the reason for this enhancement of current driving capability in AHLATI, a comparis n is made f the electric fields along the channel for both AHLATI and conventional devices (Fig. 4). In comparison to the conventional device, AHLATI shows a larger field gradient near the source end of the channel, which is due to the localized pileup region produced by the tilted halo implantation. The electrons injected from the source into the channel will experience a rapid increase of electric field and do not have enough time to reach equilibrium with the applied electric field by scattering. Therefore, the electron velocity rises rapidly at the source end of the channel and it produces the velocity overshoot phenomenon. This argument was confirmed by HD simulation [9] and, in comparison to the conventional device, AHLATI shows a 20% enhancement of electron velocity at the source end of the channel. Another advantage of the AHLATI structure is the reduction of the hot-carrier effect. As shown in Fig. 4, AHLATI has a lower electric field at the drain junction where the hot-carriers are produced. We have simulated the impact ionization rate and substrate current using a HD simulator [9] which takes into consideration the nonlocal effect in impact ionization. The predicted peak substrate currents are at least an order of magnitude less than those of the conventional devices.

In conclusion, we have introduced a new structural concept for 0.1-μm MOSFET's (AHLATI) which aids considerably in suppressing short-channel and hot-carrier effects while enhancing the current driving capability. AHLATI is unique in having an asymmetric channel profile and can be readily fabricated by utilizing large-angle-tilt implantation to locate the peak of the localized pileup region next to the source junction at the Si/SiO_2 interface. This new concept should enable MOSFET devices to be more successfully scaled to sub-0.1-μm dimensions.

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